02-27-07

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2186
Examiner: Ryan A. Dare

In re Application of:	Peter B. Criswell
Title:	System and Method for Detecting and Correcting Errors in a Control System
Serial No.:	10/675,841
Filed:	September 30, 2003
Docket No.:	RA 5635
Customer No.	27516

Date: February 16, 2007

MS Appeal Brief – Patents
Commissioner of Patents
P O Box 1450
Alexandria, VA 22313-1450

APPELLANT'S AMENDED BRIEF TRANSMITTAL

Sir:

Transmitted herewith is an Appellant's Amended Brief for this application. Applicant is other than a small entity.

We are transmitting herewith the attached:

- Appellant's Amended Brief Filed Under 37 C.F.R. 1.193 (d) in Triplicate.

FEE PAYMENT

Applicant believes no fee is required. If any additional fee is required, charge Account No. 19-3790.

A duplicate of this transmittal is attached.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited in the United States Postal Service as first class mail in an envelope addressed to: MS Appeal Brief – Patents, Commissioner of Patents, Alexandria, VA 22313-1450 on December 4, 2006.

Beth L. McMahon
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Beth L McMahon
Signature

February 16, 2007
Date of Signature

APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES
Group Art Unit: 2186
Examiner: Ryan A. Dare

Customer Assignment No.: 027516 February 16, 2007
Serial No.: 10/675,841
Filed: September 30, 2003
In re Application of: Peter B. Criswell
Title: SYSTEM AND METHOD FOR DETECTING AND CORRECTING ERRORS IN A CONTROL SYSTEM
Docket No.: RA-5635

APPELLANT'S AMENDED BRIEF

MS Appeal Brief - Patents
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P.O. Box 1450
Alexandria, VA 22313-1450

This brief is being submitted on February 16 in response to a Notification of Non-Compliant Appeal Brief under 37 CFR §41.37 dated 1/18/2007. In that Notification, Applicant's Appeal Brief filed on December 4, 2006 was deemed to be non-compliant for failing to contain the required headings. Additionally, the claimed invention was not mapped to independent Claims 12 and 26. In accordance with this Notification, this Amended Appeal Brief includes all required headings. This Brief further maps the invention to independent Claims 12 and 26. Therefore, it is respectfully submitted that this Amended Appeal Brief complies with all requirements of 37 CFR §41.37.

This Amended Appeal Brief is being filed within one month of the Notification of Non-Compliant Appeal Brief dated 1/18/2007. It is therefore believed no extension of time is required to enter this Brief. However, if an extension is required, please consider this a petition therefore and charge the extension fee to deposit account number 19-3790 along with any additional fees required to enter these papers. Appellant requests that this amended Appeal Brief be made of record and fully considered.

CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box MS Appeal Brief - Patents, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below:

Beth L McMahon — **February 16, 2007**
(Beth McMahon)

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Real Party In Interest

The real party in interest is Unisys Corporation, with an address as follows:

Unisys Corporation
Township Line and Union Meeting Roads
Blue Bell, Pennsylvania 19424

Unisys Corporation is the real party in interest through an assignment from the inventor of his entire interest, recorded on 9/30/2003 in the USPTO at Reel/Frame 014606/0270.

Related Appeals and Interferences

There are no pending appeals or interferences related to the subject Appeal.

Status of Claims

Claims 1-4 and 6-37 remain pending, and stand finally rejected.

Status of Amendments

A first amendment was submitted on February 1, 2006 to amend Claims 1, 12, 17, 18, 26, and 27, and to cancel Claim 5, of originally presented Claims 1-37. This amendment has been entered.

No further amendments have been submitted or entered.

A clean copy of Claims 1-4 and 6-37, as amended, is provided as Appendix A.

Summary of Claimed Subject Matter

Applicant's invention provides a way to add check bits to a storage device such as a control store RAM without increasing the width of that storage device. According to the invention, Applicant's storage device is part of a control circuit such as a logic sequencer. This control circuit controls the operation of one or more other circuits, such as an arithmetic logic unit (ALU) or an instruction decoder of an instruction processor.

As is known in the art, a logic sequencer such as the one that may include the current invention generally operates as follows. An address is applied to a control store RAM. Some of the signals read from that control store RAM may be used to control the operation of another circuit, such as an ALU. Other signals retrieved from the control store RAM may be used to control the logic sequencer itself during a next clock cycle. For instance, some of the signals read from the control store RAM may be used to generate a new address that will be used to retrieve signals from the control store RAM during the next clock cycle, and so on. In this manner, the sequencer not only controls another circuit, but it also generates signals that are used to control its own operation during a future clock cycle.[1]

In the foregoing manner, during a given clock cycle, a set of data signals is read from an addressable location of Applicant's storage device, which is part of a control circuit similar to that described above. The number of signals that is

[1] See Applicant's Specification ("Specification") p. 4 lines 3-15.

retrieved is determined by the width of the storage device. Some of these retrieved data signals are used to control another circuit, such as an ALU. Other data signals may be used for "self-control" of the control circuit itself during future clock cycles.

When a set of data signals is read from Applicant's storage device, the number of those signals required to perform "self-control" functions varies based on which operations are going to be performed during the next clock cycle. In many cases, the number of signals needed for self-control is relatively small such that some signals in the data set are unused.[2] The number of signals required to control the other circuit (e.g., the ALU) also varies. For instance, if the other circuit is performing a less complex operation, some of the signals that would otherwise be provided to control this other circuit remain unused.[3] In either of these cases, unused signals may be employed for another purpose. According to the invention, these unused signals are used as Error Correction Code (ECC) check bits that can detect, and in many cases, correct, errors occurring within that set of data signals.[4]

When a set of data signals is read from the storage device of the control circuit, a mode indicator is also retrieved along with these signals to indicate whether otherwise unused signals in that data set are being used as check bits. Specifically, if the mode indicator is set to a first mode, all data signals in the set are needed for control purposes. If, however, the mode indicator is set to a

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[2] This occurs, for example, when an external source is providing signals to control operation of the control circuit during clock cycles when the control circuit is operating as a "slave". See Specification p. 4 line 19–26.
[3] Specification p. 15 line 22 – p. 16 line 2.

second mode, some of the data signals in that set are not needed to perform control. These otherwise unused data signals are therefore employed as check bits to detect, and possibly correct, errors occurring within the set of data signals.[5]

As may be appreciated from the foregoing, Applicant's invention assigns a dual purpose to some bits of a storage device. In a first mode, these bits are used as control signals. In a second "ECC" mode, the bits are instead used to provide ECC protection for the set of data signals in which they are included.[6] This allows ECC protection to be added to the system without increasing the width of the storage device. This is important since providing enough dedicated ECC check bits to protect data read from a 300-bit wide control store RAM would increase the RAM width by approximately 40 bits, which is considered unacceptable for some applications.[7]

Next, the foregoing discussion may be applied to the exemplary embodiment of Applicant's Figure 4. In Figure 4, Applicant's storage device is shown as control store RAM 300. When a set of data signals is read from this storage device, this set is captured along with the ECC mode indicator[8] by register L0 304. If the circuit is operating in the first mode as determined by the ECC mode indicator, no ECC protection is provided. Therefore, data signals flow from register L0 304, through select circuits 454 and 458, onto lines 428, and through ECC complement logic 426. ECC complement logic 426 is

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[4] Specification p. 5 lines 1-7.
[5] Specification p. 15 line 20 – p. 16 line 2.
[6] Specification p. 14 lines 17-22.
[7] Specification p. 3 lines 12-24.

configured via AND gates 424 and the ECC mode designator not to perform any correction. The uncorrected data signals are driven by ECC complement logic 426 onto lines 429, are captured by staging registers L1 306 and L2 308, and are then supplied to control the ALU logic 310.

Whereas some of the data signals captured by L0 register 304 during the first mode are provided to ALU logic 310 for control purposes, other signals captured by the L0 register during the same clock cycle are used for "self-control". For example, some signals are directed to branch logic 326 for use in generating the next address that is to be provided to control store RAM 300 during the next clock cycle.

In contrast to the first mode of operation described above, the circuit of Figure 4 may also operate in a second ECC mode. In this second mode, the ECC mode signal on line 400 causes select circuit 405 to select some of the signals on lines 408 for use as ECC check bits rather than as control signals.[9] ECC logic 406 uses these check bits to determine whether an error occurred on any data bit provided on lines 408. If an error is detected, a corresponding complement bit is set within lines 420.[10] AND gates 424 process the complement bits 420 to generate signals that control whether ECC complement logic 426 will correct a corresponding data bit that is received on line 428.[11]

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[8] ECC mode indicator on line 400 of Figure 4.
[9] Specification p. 17 lines 3-24, for example.
[10] Specification p. 17 lines 20-24.
[11] Only those data bits that are determined to be "correctable" by the mask in the L0 Bit Register 422 will be corrected by the ECC Complement Logic 426. See, for example, Specification p. 19 lines 16–27.

When an error is corrected during the second ECC mode of operation, normal processing activities need not be interrupted at the time the error is detected. The error is simply reported, and any required recovery actions may be initiated at a later time.[12] In contrast, during the first mode of operation wherein ECC bits are not available, parity checkers 334-338 detect, but do not correct, errors such that normal processing may have to be temporarily halted to perform error recovery when an error is detected.[13]

Various aspects of Applicant's invention that are discussed above map to Applicant's Claim 1 as follows:

1. A control system, comprising:

a storage device[14] to store data signals[15] and a mode designator[16], the mode designator to select a first or a second mode of operation;

a circuit[17] coupled to the storage device to receive as control signals predetermined ones of the data signals along with the mode designator, the control signals to control operation of the circuit when the circuit is operating in the first mode[18]; and

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[12] Specification p. 17 line 25 – p. 18 line 6.
[13] Specification p. 14 lines 2-16.
[14] Control Store RAM 300 of Figure 4. See Specification p. 11 line 22 et seq.
[15] The "N-1" data signals are shown on lines 407 of Figure 4. See Specification p. 11 line 23 et seq., for example.
[16] ECC mode signal 400 of Figure 4. Specification p. 15 line 21 et. seq., for example.
[17] In the exemplary embodiment of Figure 4, this circuit includes logic that receives the signals on lines 408 for control purposes, including select circuits 302, 454, 458, and 405 and interconnecting logic such as Branch Logic 326 and ALU Logic 310. See, for example, Specification p. 12 line 15 – p. 13 line 4, p. 15 line 25 – p. 16 line 2, p. 21 lines 13-15, and p. 23 line 24 – p. 24 line 7, for instance.
[18] The first mode is selected when the ECC mode signal is inactive. See Specification p. 15 lines 22-26, for example.

Error Correction Code (ECC) logic[19] coupled to the storage device to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in the second mode[20].

[19] This logic includes Figure 4 ECC Logic 406, AND Gates 424, Select Logic 320 and 405, and ECC Complement Logic 426. See, for example, Specification p. 17 lines 3-24, p. 19 lines 19-27.

[20] When the ECC mode signal is high-active, selected ones of the data signals are used by ECC logic 406 to detect errors and generate complement control bits on lines 420 according to a selected ECC scheme. Selected ones of these complement control bits are gated by AND Gates 424 to ECC Complement Logic 426 for correction. This gating occurs only for errors that are considered correctable as determined by a mask in register 422. For instance, Specification p. 16 line 25–p. 19 line 19.

Various aspects of Applicant's invention that are discussed above map to Applicant's independent Claim 12 as follows:

12. A method of controlling a digital system, comprising:

a.) reading[21] first data signals[22] along with a mode indicator[23] from a storage device[24];

b.) interpreting[25] the first data signals as control signals to control one or more functions of the digital system if operating in a first mode[26] of operation as determined by a state of the mode indicator; and

c.) interpreting[27] the first data signals as Error Correction Code (ECC) signals if operating in a second mode[28] of operation as determined by the state of the mode indicator.

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[21] Step 500 of Figure 5. Specification p. 24 line 26.
[22] The "N-1" data signals are shown on lines 407 of Figure 4. See Specification p. 11 line 23 et seq.
[23] ECC mode signal 400 of Figure 4. Specification p. 15 line 21 et. seq.
[24] Control Store RAM 300 of Figure 4. See Specification p. 11 line 22 et seq.
[25] Step 504 of Figure 5. See Specification p. 25 lines 1-5.
[26] Specification p. 25 lines 1-5.
[27] Steps 506-508 of Figure 5. See Specification p. 25 lines 6-11.
[28] Specification p. 25 lines 6-11.

Various aspects of Applicant's invention that are discussed above map to Applicant's independent Claim 26 as follows:

26. (Once Amended) A control system having a first and second mode of operation, comprising:

storage means[29] for storing data signals[30] and a mode designator[31], a state of the mode designator selecting[32] between operation in the first mode or the second mode;

control means[33] for receiving the data signals with the mode designator, and for utilizing first ones of the data signals to affect operations of the control system when operating in the first mode; and

error means[34] for interpreting the first ones of the data signals as check bits for detecting errors occurring in second ones of the data signals when the control system is operating in the second mode.

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[29] For example, Control Store RAM 300 of Figure 4. See Specification p. 1 lines 12-17, p. 2 lines 5-14, p.11 line 22 et seq., for example.
[30] The "N-1" data signals are shown on lines 407 of Figure 4. See Specification p. 11 line 23 et seq., for example.
[31] ECC mode signal 400 of Figure 4. Specification p. 15 line 21 et. seq., for instance.
[32] Figure 5 step 502 and Specification p. 24 line 27 – p.25 line 11, for instance.
[33] Figure 4 Select Circuits 320, 454, 458, and 405 and interconnecting logic, Branch Logic 326 and ALU logic 310. See, for example, Specification p. 2 lines 7-14, p. 11 line 17–p. 12 line, p. 12 line 15-p. 13 line 4, p. 15 line 25, p. 21 lines 13-15, and p. 23 line 24–p. 24 line 7, for instance.
[34] Figure 4 ECC logic 406, AND Gates 424, Select Logic 320 and 405, and ECC Complement Logic 426. See, for example, Specification p. 17 lines 3-24, p. 19 lines 19-27.

Various aspects of Applicant's invention map to dependent means-plus-function Claims 27-36 as follows:

27. The system of Claim 26, wherein the storage means includes means for storing the mode designator[35] to control whether the control system is operating in the first or the second mode.

28. The system of Claim 26, wherein the control means includes branch means[36] for utilizing the first ones of the data signals to generate an address for the storage means.

29. The system of Claim 26, wherein the storage means is a memory including predetermined addressable locations, each storing a different respective set of the first and second ones of the data signals[37].

30. The system of Claim 29, wherein each of the predetermined addressable locations within the memory includes means for storing a mode designator for controlling whether the control system operates in the first or the second mode when the first and the second ones of the data signals stored at the addressable location are read from the memory[38].

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[35] Figure 4 Control Store RAM 300 provides N signals on lines 302, which, in turn, provide the N-1 data signals shown on lines 407 and the ECC mode signal shown on line 400. Specification p. 15 lines 21-22, for example.
[36] Figure 4 Branch Logic 326. Specification p. 15 lines 4-6, for instance.
[37] Figure 4 Control Store RAM 300, for example.
[38] Specification p. 15 lines 20-26, for example

31. The system of Claim 30, wherein the error means includes means for correcting an error[39] detected on predetermined ones of the second ones of the data signals when the control system is operating in the second mode.

32. The system of Claim 31, and further including means for providing corrected ones of the second ones of the data signals to the control means for use in affecting the operations of the control system[40].

33. The system of Claim 31, and further including parity detection means for detecting parity errors within the first or the second ones of the data signals[41].

34. The system of Claim 33, wherein the parity detection means includes means for detecting uncorrected parity errors remaining within the second ones of the data signals[42].

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[39] Figure 4 ECC Logic 406, AND Gates 424, and ECC Complement Logic 426. Specification p. 17 lines 3-24, p. 20 lines 1-7, for instance.
[40] Figure 4 Nets 429, Registers 306 and 308. Specification p. 20 lines 5–10, for instance.
[41] Figure 4 L0 Register 304, L1 Register 306, L2 Register 308, Parity Checkers 334, 336 and 338, L0 Mask Register 450, L0 Bit Register 422, AND Gates 424, ECC Complement Logic 426, Select Logic 454 and 458. For example, Specification p. 14 lines 2-16, p. 20 lines 8-14.
[42] Figure 4 L0 Register 304, L1 Register 306, L2 Register 308, Parity Checkers 334, 336 and 338, L0 Mask Register 450, L0 Bit Register 422, AND Gates 424, ECC complement Logic 426, Select Logic 454 and 458. For instance, see Specification p. 18 line 7–p. 20 line 14.

35. The system of Claim 33, and further including maintenance means[43] for performing error recovery actions within a first time period for errors detected by the parity detection means and, for errors detected by the error means, performing error recovery actions any time the control system is appropriately configured.

36. The system of Claim 26, and further including means for programmably selecting[44] the first ones of the data signals.

37. The system of Claim 31, and further including means for programmably selecting the predetermined ones of the second ones of the data signals[45].

[43] For example, Figure 1 Maintenance Processor 40 and Scan Interface 42. Specification p. 8 lines 20-25, p. 14 lines 7-16, p. 17 line 25–p. 18 line 6, p. 20 lines 13-14.
[44] For example, Figure 1 Maintenance Processor 40 and Scan Interface 42, Figure 4 L0 Mask Register 450, AND Gates 451, Select Circuit 405. Specification p. 5 lines 22-27, p. 8 lines 20-25, p. 17 lines 8-14, p. 21 line 22–p. 23 line 5, p. 24 line 8-21.
[45] For example, Figure 1 Maintenance Processor 40 and Scan Interface 42, Figure 4 L0 Mask Register 450, AND Gates 451, L0 Bit Register 422, Control Store RAM 300, Select Circuit 405. Specification p. 5 lines 22-27, p. 8 lines 20-25, p. 14 lines 7-16, p. 19 line 8-p. 20 line 14.

Grounds of Rejection to be Reviewed on Appeal

I. Whether Claims 1-4 and 6-37 are anticipated under 35 USC §102(b) by U.S. Patent Number 4,201,337 to Lewis et al. (hereinafter, "Lewis").

This ground of rejection may be divided into the following sub-issues A-D:

A.) Whether the Lewis ECC/BP mode signal teaches Applicant's mode designator.

B.) Whether Lewis teaches Applicant's storage device.

C.) Whether Lewis teaches signals that are used to control a circuit coupled to the storage device during a first mode, and that are instead interpreted by ECC logic as check bits during a second mode.

D.) Whether Lewis teaches Applicant's circuit that is coupled to a storage device and that operates in a first mode to receive as control signals the predetermined signals.

Argument

I. Whether Claims 1-4 and 6-37 are anticipated under 35 USC §102(b) by U.S. Patent Number 4,201,337 to Lewis et al.

Before considering this issue in detail, the Lewis system is summarized for discussion purposes. Lewis describes an error detection and correction (EDC) circuit that operates in either an error correction code (ECC) mode or a byte parity (BP) mode. When the EDC circuit has been configured to operate in ECC mode, the circuit uses a Hamming code to generate ECC check bits on data being stored to RAM. These check bits can then be used to detect, and possibly correct, errors when the data is later read from RAM. When the EDC circuit is instead configured to operate in BP mode, the EDC circuit is used to generate or verify byte parity on the data.[46] The mode of operation is determined by a signal applied to an ECC/BP terminal of the Lewis circuit.[47]

The Lewis system was developed at a time when data processing systems were constructed primarily of discrete components. The dual-mode operation of the Lewis EDC circuit was provided to fulfill "...the need to limit the number of LSI chip-types in a data processing system."[48] In other words, at one place in a given design, an instance of the EDC circuit (e.g., one LSI component) could be used in BP mode, and at a different point in the same design, a different instance of this same circuit (e.g., a different chip) could be configured

[46] Lewis column 1 lines 50-54.
[47] Lewis Figure 2, ECC/BP terminal, and column 6 lines 5-7 and 38-39.
[48] Lewis column 1 lines 64-65.

in ECC mode. In this manner, the same chip-type was used in two different ways, thereby minimizing the number of chip-types maintained in a manufacturing inventory. This is described in reference to Lewis Figure 1, wherein instance 30a of the EDC circuit is said to be configured in ECC mode, and instances 30b-30f of this circuit are described as being used in BP mode.[49]

It does not appear from Lewis that the same instance of the EDC circuit can be configured to operate in ECC mode at some times and to operate in BP mode at other times. That is, a given instance of an EDC circuit is configured to always operate in BP mode, or to always operate in ECC mode.

With the foregoing summary of the Lewis EDC circuit available for discussion purposes, the sub-issues set forth above within respect to Issue I are considered in turn.

A.) Whether the Lewis ECC/BP mode signal teaches Applicant's mode designator.

Lewis is first cited in the Final Rejection of the Claims dated 4/20/2006 (hereinafter, "Final Rejection".) In that Final Rejection, the Examiner does not specifically state which aspect of Lewis teaches Applicant's mode designator. However, the Examiner does state that Applicant's first mode is taught by the

[49] Lewis column 3 lines 29-32 and 51-53, and column 4 lines 9-12.

Lewis BP mode, and Applicant's second mode is taught by the Lewis ECC mode.[50]

From the foregoing, it may be inferred that the Examiner is asserting that the signal in Lewis that selects between ECC and BP modes teaches Applicant's mode designator which selects Applicant's mode. That is, the Examiner is asserting that the signal that drives the Lewis ECC/BP control input terminal of the EDC circuit, as shown in Lewis Figure 2, teaches Applicant's mode designator .[51] For discussion purposes, the Lewis signal that drives the ECC/BP control input terminal will hereinafter be referred to as the ECC/BP signal.

The Lewis ECC/BP signal is not described in any detail in Lewis. It is probable that, for any given EDC circuit instance, the ECC/BP input terminal is tied to either a high or a low voltage level.[52] This conclusion may be drawn from the fact that Lewis describes a given EDC circuit instance as always being used in ECC mode, or always being used in BP mode. Lewis never describes the same instance of the EDC circuit as being used in ECC mode at some times and in BP mode at other times. If fact, it seems quite improbable that an instance of an EDC circuit could be used in both modes since the way in which the circuit is interconnected to surrounding circuit elements when used in ECC mode is quite different from the way the circuit is connected when used in BP mode. This may

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[50] Final Rejection of the Claims dated 4/20/2006, hereinafter "Final Rejection", p. 2 last sentence.
[51] Lewis column 6 lines 5-6 and 38-39.
[52] Another possible explanation for the way in which the ECC/BP signal is generated is that it is somehow provided by control circuit 24. This control circuit, which is mentioned only briefly, is said to control the sequencing of each components of the system, as set forth in Lewis column 6 lines 2-5.

be appreciated by comparing the ECC-mode interconnection shown in Figure 5 to the BP-mode interconnection of Figure 6.

Regardless of how the Lewis ECC/BP mode signal is generated, nothing in Lewis describes this signal as being stored, and then provided, by any storage device, as is claimed by Applicant's Claim 1[53]. In fact, because the Lewis ECC/BP mode signal appears to remain at a constant voltage level for any given circuit instance, using a storage device to store, and then to supply, this signal would appear entirely unnecessary.

Further to the foregoing point, nothing in Lewis describes the Lewis ECC/BP mode signal as being stored by a storage device that also stores some other data signals, as is claimed Applicant's Claim 1[54]. Because Lewis does not teach Applicant's mode designator that is stored in a storage device along with other signals, Lewis does not teach each and every element of Applicant's representative Claim 1.

B.) Whether Lewis teaches Applicant's storage device.

From the discussion set forth above, it follows that Lewis does not teach Applicant's storage device for storing a mode designator and data signals. Nothing in Lewis shows, describes, or in any way alludes to, a storage device that stores an ECC/BP signal that is provided to the ECC/BP input terminal of the

[53] Applicant's Claim 1 lines 2 and 5.
[54] Applicant's Claim 1 line 2.

EDC circuit. Moreover, nothing in Lewis in any way alludes to a storage device that stores an ECC/BP signal and that also stores data signals.

C.) Whether Lewis teaches signals that are used to control a circuit when that circuit is operating in first mode, and that are instead used as ECC check bits by ECC logic during a second mode.

The Examiner states that the Lewis BP mode teaches Applicant's first mode, and the Lewis ECC mode teaches Applicant's second (ECC) mode.[55]

From the language of Applicant's Claim 1, when Applicant's circuit is running in the second mode, ECC logic interprets some of the data signals as check bits that are used to detect, and possibly correct, any errors occurring on the data signals.[56] When Applicant's circuit is instead operating in first mode, those same signals are no longer used as check bits, but instead are interpreted as control signals that control operation of a circuit that is coupled to the storage device.[57] Lewis does not teach this aspect of the invention, as may be appreciated by the following observations.

First, only an instance of the Lewis circuit that is operating in ECC mode interprets signals as check bits. A Lewis circuit instance that is instead operating in BP mode does not generate, receive, or otherwise use, check bits. For example, Lewis Figure 5 shows how an EDC circuit instance is configured to operate in ECC mode. In this configuration, check bits are generated and

[55] Final Rejection p. 2 last sentence.

received on bus 38.[58] In contrast, the BP mode adaptation of a circuit instance is illustrated by Lewis Figure 6. In this configuration, the circuit does not generate, receive, or in any other way use, check bits as is described in the Lewis discussion of Figure 6.[59]

Secondly, it may again be observed that a single instance of the Lewis EDC circuit always operates in ECC mode, or always operates in BP mode. An EDC circuit instance does not operate some of the time in ECC mode and some of the time in BP mode. This may be appreciated by considering that an EDC circuit instance may be connected according to the ECC configuration illustrated in Figure 5, or may instead be connected according to the BP configuration shown in Figure 6. Nowhere does Lewis describe or suggest any way for an EDC circuit instance to be configured to operate in one mode some of the time, and another mode at other times.

The two observations set forth above may be summarized as follows:

a.) In Lewis, whenever signals are being interpreted as check bits, they are being interpreted by an EDC circuit instance operating in ECC mode; and

b.) The EDC circuit instance that is receiving the check bits will never operate in a mode other than ECC mode.

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[56] Claim 1 lines 8-10.
[57] Claim 1 lines 6-7.
[58] See, for example, Lewis column 7 lines 11-13, 50-51, and 60-66.
[59] See Lewis column 10 line 7 – column 11 line 2 regarding Figure 6.

The foregoing points lead to the conclusion that, in Lewis, signals interpreted as check bits by a circuit operating in the second ECC mode are never used, or even received, by any circuit that is configured to operate in a first BP mode. Thus, Lewis does not teach any signals that are used some of the time by a circuit operating in a first BP mode, and that are used at other times by a circuit operating in ECC mode. To re-state, Lewis does not teach Applicant's signals used to control a circuit when that circuit is operating in a first mode, and that are instead used as ECC check bits when that circuit is operating in a second mode.[60]

D.) Whether Lewis teaches Applicant's circuit that operates in a first mode to receive predetermined signals as control signals, and that further operates in a second mode during which the predetermined signals are interpreted as ECC check bits.

The Examiner cites the following passage from the Lewis "Background of the Invention" section as teaching Applicant's circuit of Claim 1 lines 4-7:

> "Furthermore, the circuit must also be capable of delivering control signals to each of the LSI data chips which receive slices of data so that each of the data chips may be constructed identically, even though they may be controlled individually."[61]

[60] Applicant's Claim I lines 4-7 and 9-10.
[61] Lewis column 1 lines 37-41 as cited on p. 3 line 3 of the Final Rejection.

This cited passage of Lewis is not discussing any particular circuit in the Lewis system, but rather is making a general reference to characteristics that are desirable in a system for detecting or corrected data errors. Thus, it is difficult to address the Examiner's assertion in regards to this aspect of the invention.

Rather than attempting to address the Examiner's specific assertion regarding this element of the Claim, general observations may be made regarding why Lewis cannot possibly teach Applicant's circuit element that is described in lines 4-7 of Claim 1.

First, Applicant's circuit is described as operating in the first mode some of the time and as operating in the second mode at other times.[62] As discussed in detail above, in Lewis, the same EDC circuit instance never operates in a first BP mode some of the time and in a different ECC mode at other times. Moreover, no other circuit in Lewis operates in BP mode some of the time and in ECC mode at other times. Thus, there is no circuit in Lewis that could possibly teach Applicant's circuit of Claim 1.

Moreover, Applicant's Claim 1 describes a circuit that operates in first mode and that never-the-less receives signals that would be interpreted during a second mode of operation as ECC check bits.[63] As previously described, in Lewis, the signals used as ECC check bits are never provided to any circuit instance that ever operates in "first" BP mode. Therefore, Lewis doesn't teach Applicant's circuit that operates in a first mode and that receives the same

[62] Claim 1 lines 6-7 and 10.
[63] Claim 1 lines 4-5 and 9.

signals that are otherwise interpreted as check bits during a second operating mode.[64]

Finally, Applicant's circuit is described as being coupled to the storage device that stores the mode designator.[65] As set forth above, Lewis does not describe any storage device storing the ECC/BP mode signal. Therefore, Lewis does not teach a circuit that is coupled to such a storage device.

To summarize, Lewis fails to teach at least the following aspects of Applicant's representative Claim 1:

1. A storage device that stores a mode designator;
2. A storage device that stores a mode designator and data signals;
3. Signals that are used to control a circuit coupled to the storage device during a first mode, and that are interpreted by ECC logic as check bits during a second mode; and
4. Applicant's circuit that is coupled to the storage device, and that operates in both a first mode and a second mode. During first mode, the circuit uses as control signals the same signals that are otherwise interpreted as ECC signals when that circuit is operating in the second mode.

For at least the foregoing reasons, Lewis does not teach each and every element of representative independent Claim 1. The remaining independent Claims 12 and 26 include aspects that are similar to those set forth in regards to

[64] Claims 1 lines 4-7 and 9-10.

Claim 1. In a manner similar to that described above, Lewis does not teach each and every element of these additional independent Claims. Likewise, Lewis does not teach each and every element of the various dependent Claims that each depends from a respective one of the independent Claims. Therefore, the Examiner has failed to set forth a prima facie case of anticipation for Applicant's pending Claims 1-4 and 6-37 as required by 35 USC §102(b).

[65] Claim 1 lines 2 and 4.

Conclusion and Request for Relief

Applicant's Claims 1-4 and 6-37 are patentable over Lewis. This reference does not teach each and every element of Applicant's independent Claims. The Examiner has failed to set forth a prima facie case of anticipation under 35 USC §102(b) in regards to the Claims. It is therefore respectfully requested that the rejection of the Claims be overturned, and the Claims be passed to issue.

Respectfully submitted,

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Claims Appendix

Presented is a clean set of Claims 1-4 and 6-37 as last amended February 1, 2006.

1.(Once Amended) A control system, comprising:

a storage device to store data signals and a mode designator, the mode designator to select a first or a second mode of operation;

a circuit coupled to the storage device to receive as control signals predetermined ones of the data signals along with the mode designator, the control signals to control operation of the circuit when the circuit is operating in the first mode; and

Error Correction Code (ECC) logic coupled to the storage device to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in the second mode.

2. (Original) The system of Claim 1, wherein the storage device is a memory having multiple addressable storage locations, each storing a different respective set of data signals.

3. (Original) The system of Claim 2, wherein each of the addressable storage locations includes circuits to store a respective mode designator to control

whether the circuit operates in the first or the second mode after the data signals stored at the addressable storage location are read from the memory.

4. (Original) The system of Claim 3, wherein the circuit includes branch logic to utilize the predetermined ones of the data signals stored at an addressable storage location to generate a next address for addressing the memory if the mode designator stored at the addressable storage location indicates the circuit will operate in the first mode.

5. (Canceled)

6. (Original) The system of Claim 1, wherein the circuit includes logic to provide one or more functions of an instruction processor.

7. (Original) The system of Claim 1, and further including a programmable storage device coupled to the circuit to select the predetermined ones of the data signals.

8. (Original) The system of Claim 1, and further including at least one parity circuit coupled to the storage device to determine whether a parity error occurred on any of a predetermined set of the data signals.

9. (Original) The system of Claim 8, wherein the at least one parity circuit includes a circuit to determine whether a parity error occurred on the

predetermined set of the data signals when the circuit is operating in the second mode.

10. (Original) The system of Claim 1, wherein the ECC logic is coupled to ECC complement logic to correct errors in the data signals that are detected by the ECC logic when operating in the second mode.

11. (Original) The system of Claim 10, and further including logic coupled to the ECC complement logic to provide the data signals to the circuit for use as control signals after any errors detected by the ECC logic have been corrected.

12. (Once Amended) A method of controlling a digital system, comprising:

a.) reading first data signals along with a mode indicator from a storage device;

b.) interpreting the first data signals as control signals to control one or more functions of the digital system if operating in a first mode of operation as determined by a state of the mode indicator; and

c.) interpreting the first data signals as Error Correction Code (ECC) signals if operating in a second mode of operation as determined by the state of the mode indicator.

13. (Original) The method of Claim 12, and further including:

reading second data signals from the storage device; and

using the ECC signals to detect errors in the second data signals if operating in the second mode of operation.

14. (Original) The method of Claim 13, wherein the storage device is a memory, and wherein the first and second data signals are stored at a same addressable location within the memory.

15. (Original) The method of Claim 14, wherein multiple memory addresses each stores different respective first and second data signals.

16. (Original) The method of Claim 15, and further including using the first data signals to generate a next address for addressing the memory when operating in the first mode of operation.

17. (Once Amended) The method of Claim 15, and further including:

reading one of the multiple memory addresses; and

interpreting at least one of the second data signals as the mode indicator to indicate whether operation is occurring in the first or the second mode of operation.

18. (Once Amended) The method of Claim 17, and including repeating the steps of Claim 17 for each of multiple memory addresses.

19. (Original) The method of Claim 13, and further including, correcting an error if the error is detected in predetermined ones of the second data signals.

20. (Original) The method of Claim 19, and further including programmably selecting the predetermined ones of the second data signals.

21. (Original) The method of Claim 12, and further including programmably selecting the first data signals.

22. (Original) The method of Claim 13, and further including interpreting one or more of the second data signals as control signals to control an arithmetic logic unit of an instruction processor.

23. (Original) The method of Claim 13, an further including using parity bits to detect a parity error occurring within the first or the second data signals.

24. (Original) The method of Claim 23, and further including:

reporting any error detected using the ECC signals; and

reporting any error detected using the parity bits.

25. (Original) The method of Claim 24, and further including:

servicing any error detected by the ECC signals at a time that is optimal for the digital system; and

servicing any error detected using the parity bits substantially immediately.

26. (Once Amended) A control system having a first and second mode of operation, comprising:

storage means for storing data signals and a mode designator, a state of the mode designator selecting between operation in the first mode or the second mode;

control means for receiving the data signals with the mode designator, and for utilizing first ones of the data signals to affect operations of the control system when operating in the first mode; and

error means for interpreting the first ones of the data signals as check bits for detecting errors occurring in second ones of the data signals when the control system is operating in the second mode.

27. (Once Amended) The system of Claim 26, wherein the storage means includes means for storing the mode designator to control whether the control system is operating in the first or the second mode.

28. (Original) The system of Claim 26, wherein the control means includes branch means for utilizing the first ones of the data signals to generate an address for the storage means.

29. (Original) The system of Claim 26, wherein the storage means is a memory including predetermined addressable locations, each storing a different respective set of the first and second ones of the data signals.

30. (Original) The system of Claim 29, wherein each of the predetermined addressable locations within the memory includes means for storing a mode designator for controlling whether the control system operates in the first or the second mode when the first and the second ones of the data signals stored at the addressable location are read from the memory.

31. (Original) The system of Claim 30, wherein the error means includes means for correcting an error detected on predetermined ones of the second ones of the data signals when the control system is operating in the second mode.

32. (Original) The system of Claim 31, and further including means for providing corrected ones of the second ones of the data signals to the control means for use in affecting the operations of the control system.

33. (Original) The system of Claim 31, and further including parity detection means for detecting parity errors within the first or the second ones of the data signals.

34. (Original) The system of Claim 33, wherein the parity detection means includes means for detecting uncorrected parity errors remaining within the second ones of the data signals.

35. (Original) The system of Claim 33, and further including maintenance means for performing error recovery actions within a first time period for errors detected by the parity detection means and, for errors detected by the error means, performing error recovery actions any time the control system is appropriately configured.

36. (Original) The system of Claim 26, and further including means for programmably selecting the first ones of the data signals.

37. (Original) The system of Claim 31, and further including means for programmably selecting the predetermined ones of the second ones of the data signals.

Evidence Appendix

(None)

Related Proceedings Appendix

(None)